Patent Claims:

1. A method for the detection and/or correction of memory access errors in a processor system, wherein test data (P) is stored inside a memory (4) in addition to data (D) which is to be secured, using the latter data (D), c h a r a c t e r i z e d in that in addition to the data (D) to be secured, the data's addresses are taken into account when generating the test data (P),.

2. The method as claimed in claim 1, c h a r a c t e r i z e d in that data (D) to be secured is transmitted jointly with its associated test data (P) to a data receiver, and the test data (P) is evaluated for error detection only after the data transfer.

3. The method as claimed in claim 1 or 2, c h a r a c t e r i z e d in that the test data (P) is evaluated for error detection in an error detection device (6) that is checked by a checking unit (32).

4. The method as claimed in claim 3, c h a r a c t e r i z e d in that further test data (P) is generated to check the error detection device (6) by way of the data (D) it supplies and by way of the data's addresses.

5. The method as claimed in claim 3 or 4, c h a r a c t e r i z e d in that the checking unit (32) produces comparative test data from data and addresses which are compared with test data (P) of the

error detection device (6) and/or with test data of a memory (4) connected to the error detection device (6).

6. The method as claimed in any one of claims 3 to 5, c h a r a c t e r i z e d in that separate bus lines (20, 22, 24) are used for the transmission of data (D), test data (P), and addresses (A) between the error detection device (6) and an application memory.

7. An electronic circuit arrangement (1, 1'), in particular for implementing the method as claimed in any one of claims 1 to 6, including an error detection device (6) connected to a processor core (2) and a memory (4),
c h a r a c t e r i z e d in that the error detection device (6) comprises a test data generator (14) which generates test data (P) for data (D) to be stored in the memory (4) by way of this data (D) and by way of its addresses.

8. The electronic circuit arrangement (1, 1') as claimed in claim 7,
c h a r a c t e r i z e d in that the error detection device (6) is connected to the memory (4) by way of a number of bus lines (20, 22, 24).

9. The electronic circuit arrangement (1, 1') as claimed in claim 8,
c h a r a c t e r i z e d in that separate bus lines (20, 22, 24) are respectively provided for data (D), test data (P), and addresses (A).

10. The electronic circuit arrangement (1, 1') as claimed in any one of claims 7 to 9,
c h a r a c t e r i z e d in that a checking unit (32) is associated with the error detection device (6).